AMENDMENTS TO THE CLAIMS:

1-4. (Canceled)

5. (Previously presented) A method of manufacturing a DRAM-incorporated semiconductor device in which a DRAM section and a logic section are formed on a semiconductor substrate that is isolated into elements, said method comprising:

forming a metal film comprising one of cobalt and nickel directly on surfaces of highly doped source-drain regions and gate regions in said DRAM section and said logic section; and

heat treating said device to react said metal film with said surfaces to concurrently form a metal silicide layer in each of said DRAM section and said logic section.

6. (Previously presented) The method of manufacturing a semiconductor device according to Claim 5, wherein said metal film is formed over an entire surface of said substrate, and wherein said heat treating comprises:

heating said device at 500-600°C;

removing unreacted metal film with a mixed solution of sulfuric acid and hydrogen peroxide; and

heating said device at 800°C.

7. (Previously presented) The method of manufacturing a semiconductor device according to Claim 6, wherein said metal film comprises cobalt.

8. (Original) The method of manufacturing a semiconductor device according to Claim 5, wherein dopant implantation into gates are carried out concurrently with formation of the source-drain regions that constitute transistors in the DRAM section and the logic section, and thereby P-N gates are formed.

9. (Previously presented) The method of manufacturing a semiconductor device according to Claim 5, further comprising:

forming a bit contact connecting said DRAM section with a bit line and a contact plug connecting to said source-drain in said logic section, said bit contact and said contact plug comprising a metal material.

10-22 (Canceled)

23. (New) A method of manufacturing a DRAM-incorporated semiconductor device in which a DRAM section including a memory cell, decoder and sense amplifier, and a logic section are formed on a semiconductor substrate that is isolated into elements, said method comprising:

forming a transistor having a source including two regions different in impurity density from each other, and a drain including two regions different in impurity density from each other in said DRAM section;

forming a p-MOS transistor having a p-type gate, a source including two regions different in impurity density from each other, and a drain including two regions different in impurity density from each other in said logic section;

forming an n-MOS transistor having an n-type gate, a source including two regions different in impurity density from each other and a drain including two regions different in impurity density from each other in said logic section;

forming a metal film comprising either cobalt or nickel directly on substantially all surfaces of highly impurity-doped regions in said DRAM section and said logic section; and

heating said device to react said metal film with said surfaces to concurrently form a metal silicide layer in each of said DRAM section and said logic section.